IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
BUSSON ET AL.

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **TUNER OF THE TYPE HAVING ZERO INTERMEDIATE FREQUENCY AND CORRESPONDING CONTROL PROCESS**

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

"EXPRESS MAIL" MAILING LABEL NUMBER EL747059025US

DATE OF DEPOSIT April 5, 2001

I HEREBY CERTIFY THAT THIS PAPER OR FEE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20031

Eric Link

(TYPED OR PRINTED NAME OF PERSON MAILING PAPER OR FEE)

(SIGNATURE OF PERSON MAILING PAPER OR FEE)

P050-hc 506.28660

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 10.

Please add new Claims 11 to 57.

11. A process for controlling a tuner having a zero intermediate frequency and comprising an analog circuit, a digital circuit, and an analog/digital conversion stage connected therebetween, the analog circuit comprising a frequency transposition stage and a first controlled-gain amplifier stage connected upstream thereof, the process comprising:

calculating an overall power of an entire signal having a plurality of channels received by the tuner during a phase of initialization;

comparing the calculated overall power in the digital circuit with a first reference value corresponding to a desired power at a predetermined location in the analog circuit;

adjusting a gain of the first controlled-gain amplifier stage based upon a deviation between the calculated overall power and the first reference value; and

selecting one of the plurality of channels during a phase of normal operation after the gain of the first controlled-gain amplifier stage has been adjusted.

12. A process according to Claim 11, wherein calculating the overall power comprises calculating an overall mean power.

13. A process according to Claim 11, wherein the desired power at the predetermined location in the analog receiver is a maximum power.

14. A process according to Claim 11, wherein the gain of the first controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated overall power and the first reference value.

15. A process according to Claim 11, wherein the analog circuit further comprises a baseband filter connected to an output of the frequency transposition stage, and a

second controlled-gain amplifier stage connected to an output of the baseband filter; and the process further comprising:

calculating a channel power of the selected channel during the phase of normal operation;

comparing the calculated channel power with a second reference value corresponding to a desired channel power desired at an input of the analog/digital conversion stage; and

adjusting a gain of the second controlled-gain amplifier stage based upon a deviation between the calculated channel power and the second reference value.

16. A process according to Claim 15, wherein calculating the channel power comprises calculating a mean channel power.

17. A process according to Claim 15, wherein the desired channel power at the input of the analog/digital conversion stage is a maximum channel power.

18. A process according to Claim 15, wherein the gain of the second controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated channel power and the second reference value.

19. A process according to Claim 15, wherein calculating the overall power of the entire signal is based upon a signal available between an output of the first controlled-gain amplifier stage and an input of the frequency transposition stage.

20. A process according to Claim 15, wherein calculating the overall power of the entire signal is performed in the digital circuit.

21. A process according to Claim 15, wherein the first controlled-gain amplifier stage comprises an attenuator for attenuating the entire signal.

22. A process for controlling a tuner having a zero intermediate frequency and comprising an analog circuit, a digital circuit, and an analog/digital conversion stage connected therebetween, the analog circuit comprising a first controlled-gain amplifier stage and a second controlled-gain amplifier stage with a frequency transposition stage connected therebetween, the process comprising:

calculating an overall power of an entire signal having a plurality of channels received by the tuner during a phase of initialization;

adjusting a gain of the first controlled-gain amplifier stage based upon a deviation between the calculated overall power and a first reference value corresponding to a desired power at a predetermined location in the analog circuit;

selecting one of the plurality of channels during a phase of normal operation after the gain of the first controlled-gain amplifier stage has been adjusted;

calculating a channel power of the selected channel during the phase of normal operation; and

adjusting a gain of the second controlled-gain amplifier stage based upon a deviation between the calculated channel power and a second reference value corresponding to a

desired channel power at an input of the analog/digital conversion stage.

23. A process according to Claim 22, wherein calculating the overall power comprises calculating an overall mean power.

24. A process according to Claim 22, wherein the desired power at the predetermined location in the analog receiver is a maximum power.

25. A process according to Claim 22, wherein the gain of the first controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated overall power and the first reference value.

26. A process according to Claim 22, wherein adjusting the gain of the first controlled-gain amplifier stage comprises comparing the calculated overall power with the first reference value.

27. A process according to Claim 22, wherein calculating the channel power comprises calculating a mean channel power.

28. A process according to Claim 22, wherein the desired channel power at the input of the analog/digital conversion stage is a maximum channel power.

29. A process according to Claim 22, wherein the gain of the second controlled-gain amplifier stage is adjusted

to minimize the deviation between the calculated channel power and the second reference value.

30. A process according to Claim 22, wherein adjusting the gain of the second controlled-gain amplifier stage comprises comparing the calculated channel power with the second reference value.

31. A process according to Claim 22, wherein calculating the overall power of the entire signal is based upon a signal available between an output of the first controlled-gain amplifier stage and an input of the frequency transposition stage.

32. A process according to Claim 22, wherein calculating the overall power of the entire signal is performed in the digital circuit.

33. A tuner having a zero intermediate frequency and comprising:

an analog circuit comprising

a first controlled-gain amplifier stage having an input for receiving an entire signal having a plurality of channels,

a signal routing circuit having an input for receiving the entire signal from said first controlled-gain amplifier stage, and

a frequency transposition stage connected to a first output of said signal routing circuit;

an analog/digital conversion stage having an input being connected to an output of said frequency transposition stage or to a second output of said signal routing circuit;

a digital circuit connected to said analog/digital conversion stage and comprising a first adjustment circuit for adjusting a gain of said first controlled-gain amplifier stage based upon comparing a calculated overall power of the entire signal with a first reference value corresponding to a desired power at a predetermined location in said analog circuit; and

a control circuit connected to said signal routing circuit for connecting the input to the second output thereof for adjusting a deviation between the calculated overall power and the first reference value during a phase of initialization, and for connecting the input to the first output thereof for selecting one of the plurality of channels during a phase of normal operation after the gain of said first controlled-gain amplifier stage has been adjusted.

34. A tuner according to Claim 33, wherein the calculated overall power comprises an overall mean power.

35. A tuner according to Claim 33, wherein the desired power at the predetermined location in the analog receiver is a maximum power.

36. A tuner according to Claim 33, wherein the gain of said first controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated overall power and the first reference value.

37. A tuner according to Claim 33, wherein said digital circuit further comprises:

a first calculator circuit for providing the calculated overall power; and

a first comparison circuit for comparing the calculated overall power with the first reference value.

38. A tuner according to Claim 33, further comprising a baseband filter connected to an output of said frequency transposition stage.

39. A tuner according to Claim 33, wherein said analog circuit further comprises a second controlled-gain amplifier stage connected to an output of said frequency transposition stage.

40. A tuner according to Claim 39, wherein said digital circuit further comprises a second adjustment circuit for adjusting a gain of said second controlled-gain amplifier stage based upon a deviation between a calculated channel power of a selected channel and a second reference value.

41. A tuner according to Claim 40, wherein the calculated channel power comprises a mean channel power.

42. A process according to Claim 40, wherein the gain of said second controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated channel power and the second reference value.

43. A tuner according to Claim 40, wherein said digital circuit further comprises:

a second calculation circuit for providing the calculated channel power during a phase of normal operation; and

a second comparison circuit for comparing the calculated channel power with the second reference value corresponding to a desired channel power at an input of said analog/digital conversion stage.

44. A tuner according to Claim 43, wherein the desired channel power is a maximum channel power.

45. A tuner according to Claim 33, further comprising a semiconductor substrate such that said analog circuit, said analog/digital conversion stage, and said digital circuit are integrated on said semiconductor substrate.

46. A satellite digital television receiver comprising:

a tuner having a zero intermediate frequency and comprising

an analog circuit comprising

a first controlled-gain amplifier stage having an input for receiving an entire signal having a plurality of channels,

a signal routing circuit having an input for receiving the entire signal from said first controlled-gain amplifier stage, and

a frequency transposition stage connected to a first output of said signal routing circuit;

an analog/digital conversion stage having an input being connected to an output of said frequency transposition stage or to a second output of said signal routing circuit;

a digital circuit connected to said analog/digital conversion stage and comprising a first adjustment circuit for adjusting a gain of said first controlled-gain amplifier stage based upon comparing a calculated overall power of the entire signal with a first reference value corresponding to a desired power at a predetermined location in said analog circuit; and

a control circuit connected to said signal routing circuit for connecting the input to the second output thereof for adjusting a deviation between the calculated overall power and the first reference value during a phase of initialization, and for connecting the input to the first output thereof for selecting one of the plurality of channels during a phase of normal operation after the gain of said first controlled-gain amplifier stage has been adjusted.

47. A satellite digital television receiver according to Claim 46, wherein the calculated overall power comprises an overall mean power.

48. A satellite digital television receiver according to Claim 46, wherein the desired power at the predetermined location in the analog receiver is a maximum power.

49. A satellite digital television receiver according to Claim 46, wherein the gain of said first controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated overall power and the first reference value.

50. A satellite digital television receiver according to Claim 46, wherein said digital circuit further comprises:

a first calculator circuit for providing the calculated overall power; and

a first comparison circuit for comparing the calculated overall power with the first reference value.

51. A satellite digital television receiver according to Claim 46, further comprising a baseband filter connected to an output of said frequency transposition stage.

52. A satellite digital television receiver according to Claim 46, wherein said analog circuit further comprises a second controlled-gain amplifier stage connected to an output of said frequency transposition stage.

53. A satellite digital television receiver according to Claim 52, wherein said digital circuit further comprises a second adjustment circuit for adjusting a gain of

said second controlled-gain amplifier stage based upon a deviation between a calculated channel power of a selected channel and a second reference value.

54. A satellite digital television receiver according to Claim 53, wherein the calculated channel power comprises a mean channel power.

55. A process according to Claim 53, wherein the gain of said second controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated channel power and the second reference value.

56. A satellite digital television receiver according to Claim 53, wherein said digital circuit further comprises:

a second calculation circuit for providing the calculated channel power during a phase of normal operation; and

a second comparison circuit for comparing the calculated channel power with the second reference value corresponding to a desired channel power at an input of said analog/digital conversion stage.

57. A satellite digital television receiver according to Claim 56, wherein the desired channel power is a maximum channel power.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's

convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

Michael W. Taylor

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorneys for Applicants